normal devices.

Chapter 6 analyses the electron-phonon interaction effects in DG MOSFETs with parallel connected gates using NEGF model. Acoustic phonon scattering and Optical phonon scattering are separately investigated. The effect of temperature on various scattering mechanisms are discussed. The on-current shows an increase with increasing temperature for DG MOSFETs with parallel connected gates in the nanometer regime. This is in contrast with larger devices, indicating that scattering effects are less predominant in the nano regime.

Chapter 7 concludes the thesis by briefly listing the main findings of the work such as the advantages of DG MOSFETs with parallel connected gates, its ability to suppress short channel effects and the effects of various scattering mechanisms in the device. A few suggestions are made on the extension of the present work that can be undertaken in future.

7 Conclusion

The Non-Equilibrium Green's Function (NEGF) formalism employing approximation techniques such as Buttiker probe method or modified scattering and correlation functions method has turned out to be able to model dissipative quantum transport in small devices. The scattering mechanisms in DG MOSFETs with parallel connected gates were analyzed using the NEGF models capable of incorporating electron-phonon interactions and surface roughness effects. The characteristics of the DG MOSFET with parallel connected gates turned out to be superior to that of a normal DG MOSFET.

References

[1] G. E. Moore. Cramming more components on to integrated circuits. *Electronics*, 38:114–117, 1965.

[2] International technology roadmap for semiconductors. *ITRS*, 2012.

[3] Meikei Ieong, Bruce Doris, Jakub Kedzierski, Ken Rim, and Min Yang. Silicon Device Scaling to the Sub-10-nm Regime. *Science*, 306(5704):2057–2060, 2004.

[4] M. Jagadesh Kumar and Ali A. Orouji. Two-Dimensional Analytical Threshold Voltage Model of Nanoscale Fully Depleted SOI MOSFET With Electrically Induced S/D Extensions. *IEEE TRANSACTIONS ON ELECTRON DEVICES*, 52(7):1568–1575, July 2005.

[5] V.P. Trivedi and J.G. Fossum. Scaling fully depleted SOI CMOS. *Electron Devices, IEEE Transactions on*, 50(10):2095–2103, Oct 2003.

[6] Wei Long, H. Ou, J.-M. Kuo, and K.K. Chin. Dual-material gate (DMG) field effect transistor. *Electron Devices, IEEE Transactions on*, 46(5):865–870, May 1999.

[7] Jean-Pierre Colinge. Multiple-gate SOI MOSFETs. *Solid-State Electronics*, 48(6):897 – 905, 2004. Silicon On Insulator Technology and Devices.

[8] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Yu Cao. Exploring sub-20nm FinFET design with Predictive Technology Models. In *Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE*, pages 283–288, June 2012.

[9] Yi Cui, Zhaohui Zhong, Deli Wang, Wayne U. Wang, and Charles M. Lieber. High Performance Silicon Nanowire Field Effect Transistors. *Nano Letters*, 3(2):149–152, 2003.

[10] Aaron D. Franklin, Mathieu Luisier, Shu-Jen Han, George Tulevski, Chris M. Breslin, Lynne Gignac, Mark S. Lundstrom, and Wilfried Haensch. Sub-10 nm Carbon Nanotube Transistor. *Nano Letters*, 12(2):758–762, 2012.

[11] K. Boucart and A.-M. Ionescu. Double-Gate Tunnel FET with high- κ gate dielectric. *Electron Devices, IEEE Transactions on*, 54(7):1725–1733, July 2007.

[12] L. Chang, S. Tang, Tsu-Jae King, J. Bokor, and Chenming Hu. Gate length scaling and threshold voltage control of double-gate MOSFETs. In *Electron Devices*

Meeting, 2000. IEDM '00. Technical Digest. International, pages 719–722, Dec 2000.

[13] G.V. Reddy and M.J. Kumar. A new dual-material double-gate (DMDG) nanoscale SOI MOSFET-two-dimensional analytical modeling and simulation. *Nanotechnology, IEEE Transactions on*, 4(2):260–268, March 2005.

[14] S.M. Ramey and D.K. Ferry. Modeling of quantum effects in ultrasmall FD-SOI MOSFETs with effective potentials and three-dimensional Monte Carlo . *Physica B: Condensed Matter*, 314(1-4):350 – 353, 2002. Proceedings of the Twelfth International Conference on Nonequilib rium Carrier Dynamics in Semiconductors.

[15] Haiyan Jiang, Sihong Shao, Wei Cai, and Pingwen Zhang. Boundary treatments in non-equilibrium Green's function (NEGF) methods for quantum transport in nano-MOSFETs . *Journal of Computational Physics*, 227(13):6553 – 6573, 2008.

[16] Xue Shao and Zhiping Yu. Nanoscale FinFET simulation: A quasi-3D quantum mechanical model using NEGF. *Solid-State Electronics*, 49(8):1435 – 1445, 2005.

[17] R. Venugopal, M. Paulsson, S. Goasguen, S. Datta, and M. S. Lundstrom. A simple quantum mechanical treatment of scattering in nanoscale transistors. *Journal of Applied Physics*, 93(9):5613–5625, 2003.

[18] Zhibin Ren, R. Venugopal, S. Goasguen, Supriyo Datta, and M.S. LUNDSTROM. nanoMOS 2.5: A two-dimensional simulator for quantum transport in double-gate MOSFETs. *Electron Devices, IEEE Transactions on*, 50(9):1914–1925, Sept 2003.

[19] H.S. Pal, D.E. Nikonov, Raseong Kim, and M.S. LUNDSTROM. Electron-phonon scattering in planar MOSFETs with NEGF. In *Silicon Nanoelectronics Workshop (SNW), 2010*, pages 1–2, June 2010.

[20] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto. Scaling theory for double-gate SOI MOSFETs. *Electron Devices, IEEE Transactions on*, 40(12):2326–2329, Dec 1993.

[21] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom, and D. Jovanovic. Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches. *Journal of Applied Physics*, 92(7):3730–3739, 2002.

[22] Sung-Dae Suk, Ming Li, Yun young Yeoh, Kyoung Hwan Yeo, Keun Hwi Cho, In Kyung Ku, Hong Cho, WonJun Jang, Dong-Won Kim, Donggun Park, and Won-Seong Lee. Investigation of nanowire size dependency on TSNWFET. In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 891–894, Dec 2007.

[23] C. Riddet, A.R. Brown, C.L. Alexander, J.R. Watling, S. Roy, and A. Asenov. 3-D Monte Carlo Simulation of the Impact of Quantum Confinement Scattering on the Magnitude of Current Fluctuations in Double Gate MOSFETs. *Nanotechnology, IEEE Transactions on*, 6(1):48–55, Jan 2007.

[24] R. Kotlyar, B. Obradovic, P. Matagne, M. Stettler, and M. D. Giles. Assessment of room-temperature phonon-limited mobility in gated silicon nanowires. *Applied Physics Letters*, 84(25):5270–5272, 2004.

[25] R. Ravishankar, G. Kathawala, U. Ravaioli, S. Hasan, and M. Lundstrom. Comparison of Monte Carlo and NEGF Simulations of Double Gate MOSFETs. *Journal of Computational Electronics*, 4(1-2):39–43, 2005.

List of publications based on the work

A part of the work reported in the thesis has been published in international journals and conferences. A partial list of publications is given below.

i. **Saji Joseph**, T. George James and Vincent Mathew, "Threshold Voltage Control through Layer Doping of Double Gate MOSFETs", *Journal of Semiconductor Technology and Science* , vol.10, No.3, pp. 240-250, September, 2010.

ii. **Saji Joseph**, T. George James and Vincent Mathew, "Transport Characteristics and Subthreshold Behavior of High-κ Dielectric Double Gate MOSFETs with Parallel Connected Gates", *Journal of Electron Devices* , vol.16, pp. 1363-1369, December, 2012.

iii. **Saji Joseph**, T. George James and Vincent Mathew, "Effect of Surface Roughness in Double Gate MOSFETs with Parallel Connected Gates", Communicated to *Journal of Electron Devices* .

iv. **Saji Joseph** and Vincent Mathew, "Scattering in Double Gate MOSFETs with Parallel Connected Gates", Communicated to *Journal of Semiconductor Technology and Science*.

v. **Saji Joseph**, T. George James and Vincent Mathew, "Effect of channel layer doping on the performance of nanoscale DG MOSFETs", *Proc. International Conference Electro-2009, Varanasi, India*, pp. 50-53, December, 2009.

vi. **Saji Joseph**, T. George James and Vincent Mathew, "Influence of Channel Layer Doping on Nano Double Gate MOSFETs", *Proc.International Conference on Nanomaterials & Nanotechnology (NANO-2010),Coimbatore, India*, Macmillan Publication (ISBN 023-033-193-9:9 780230 331938) ,13 - 16, December 2010.

vii. **Saji Joseph**, T. George James and Vincent Mathew, "Effect of unintentional charges on the performance of nanoscale DGMOSFETs", *Proc. Advanced Optoelectronic Materials and Devices, AOMD-08, Varanasi, India*, Macmillan India , December 2008.